Abstract

A frequency comparator circuit is configured to compare whether the frequency of two input signals are within a tolerance of each other. The frequency comparator circuit includes two counter circuits, an AND gate, and a frequency detector circuit that is configured to provide two reset signals. The two counter circuits are arranged to be clocked by a respective one of the two input signals, and further arranged to be reset by a respective one of the two reset signals. Further, the AND gate is arranged to perform an AND function on the overflow outputs of the first and second counter circuits to provide an status signal. If the status signal is high, the difference in frequency between the two input signals is less than the tolerance. If the status signal is low, the difference in frequency between the two input signals exceeds the tolerance.

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